ABSTRACT OF THE INVENTION

A method and structure is disclosed that are advantageous for aligning a contact plug within a bit line contact corridor (BLCC) to an active area of a DRAM that utilizes a insulated sleeve structure. A lower bulk insulator layer, a capacitor dielectric layer, a cell plate conductor layer, and an upper bulk insulator layer are formed upon a semiconductor substrate. An etch removes the cell plate conductor layer, the capacitor dielectric layer, and the lower bulk insulator layer so as to form an opening terminating within the lower bulk insulator layer. A sleeve insulator layer is deposited upon the upper bulk insulator layer and within the opening. Another etch removes the sleeve insulator layer from the bottom surface within the lower bulk insulator layer. A still further etch creates a contact hole that expose a contact. The contact can be upon a transistor gate, a capacitor storage node, or an active region on the semiconductor substrate. A conductive plug is then formed in the contact hole so as to be in electrical communication with the contact. The sleeve insulator layer electrically insulates the conductive plug from the cell plate conductor layer and self aligns the BLCC so as to improve contact plug alignment tolerances between the BLCC and the capacitor components.

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